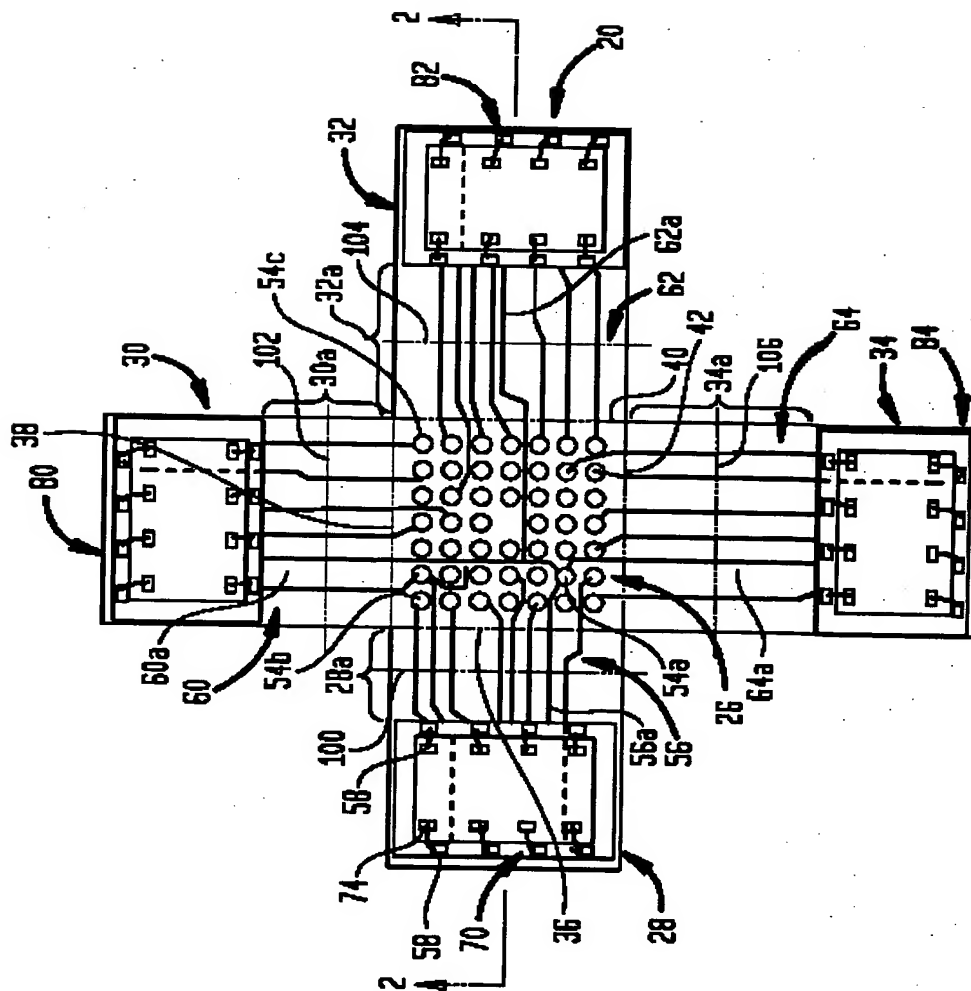


FIG. 1



**FIG. 2**

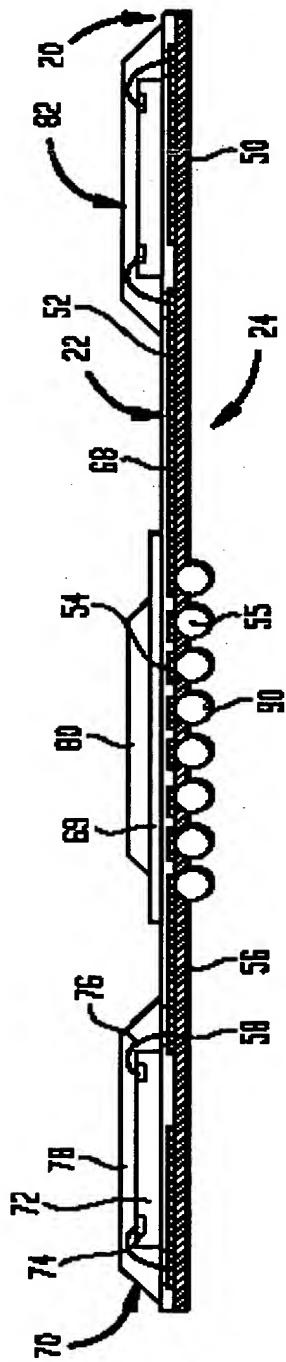


FIG. 3A

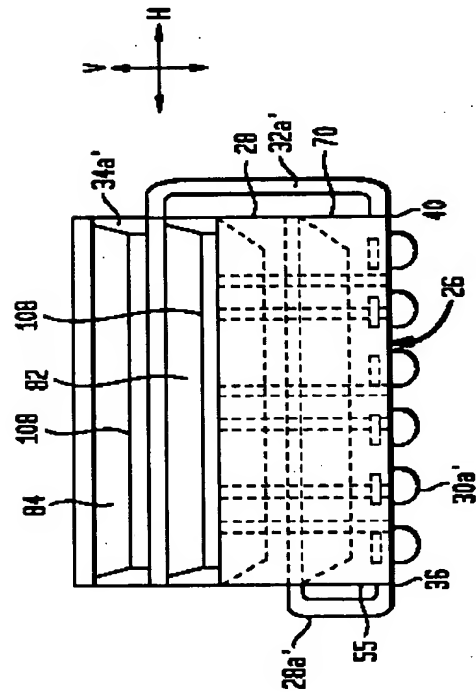


FIG. 3B

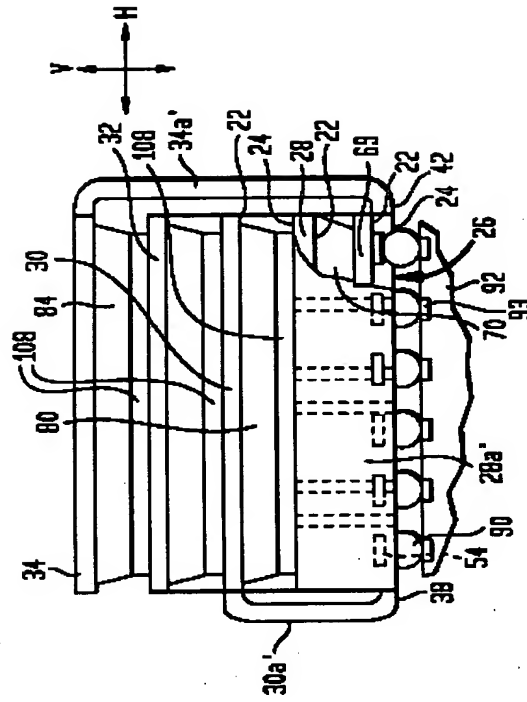


FIG. 4

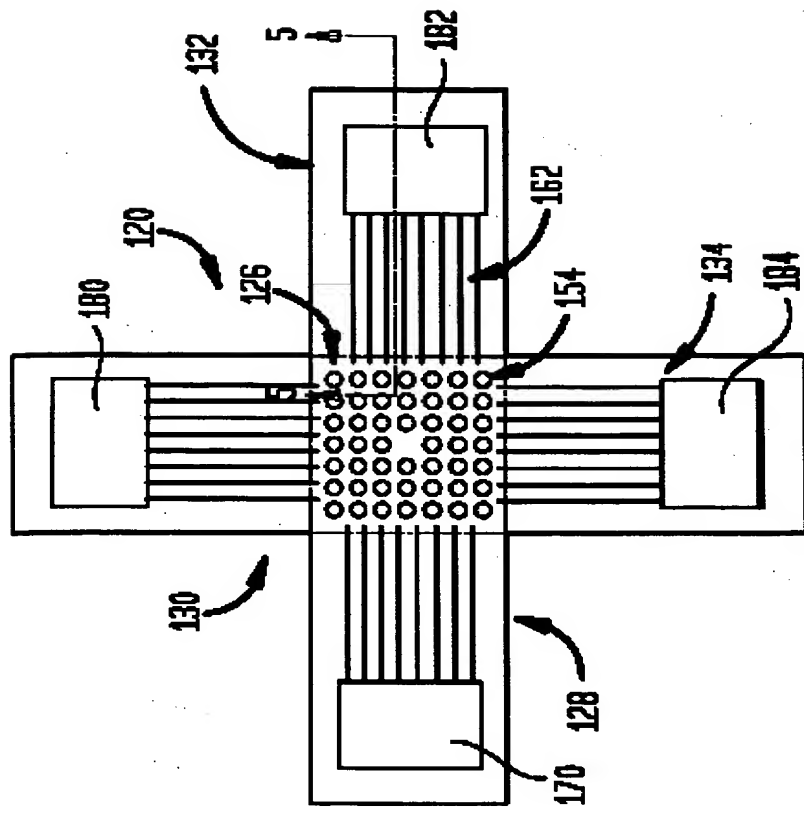


FIG. 5

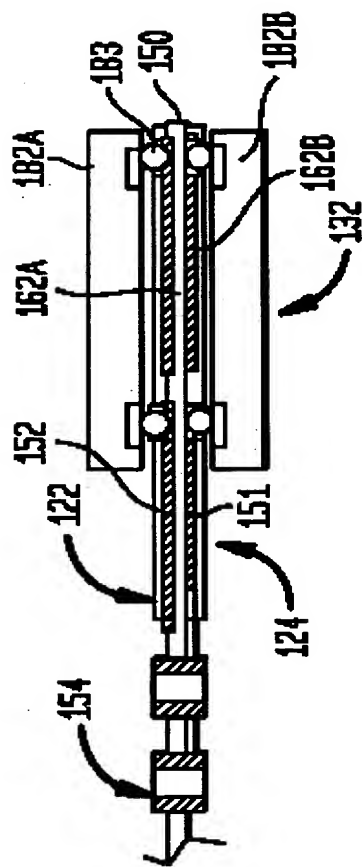




FIG. 7

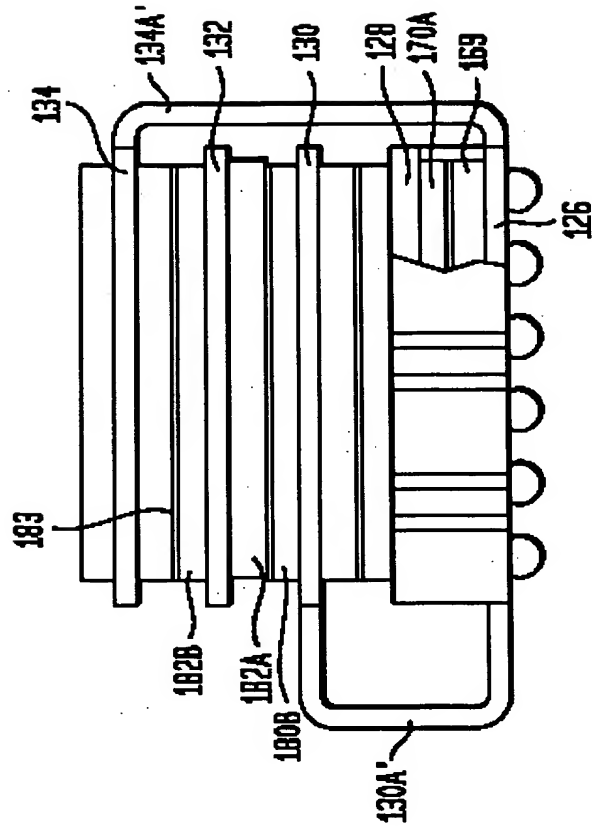


FIG. 8

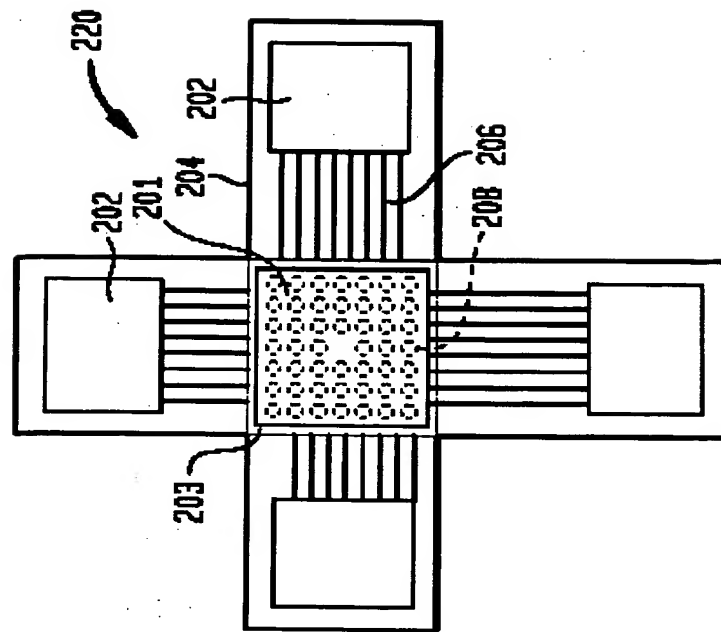
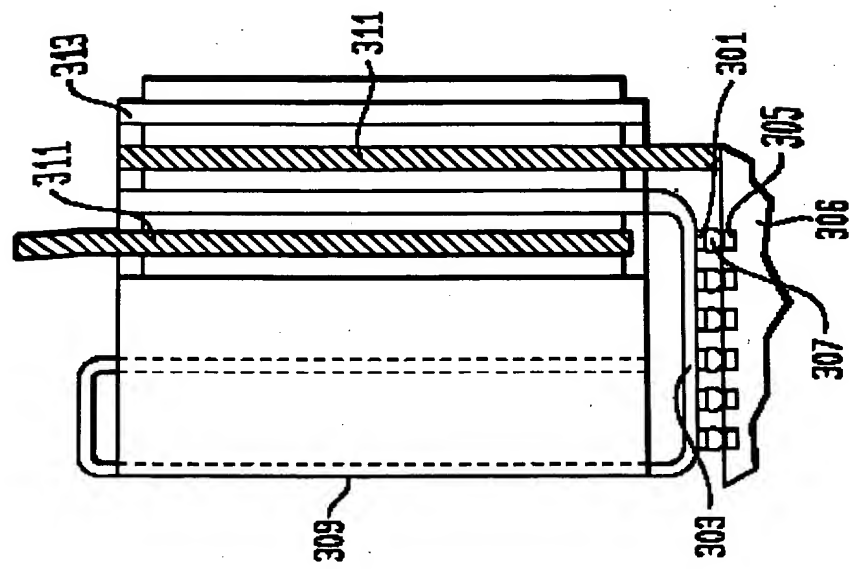




FIG. 9



**FIG. 10**

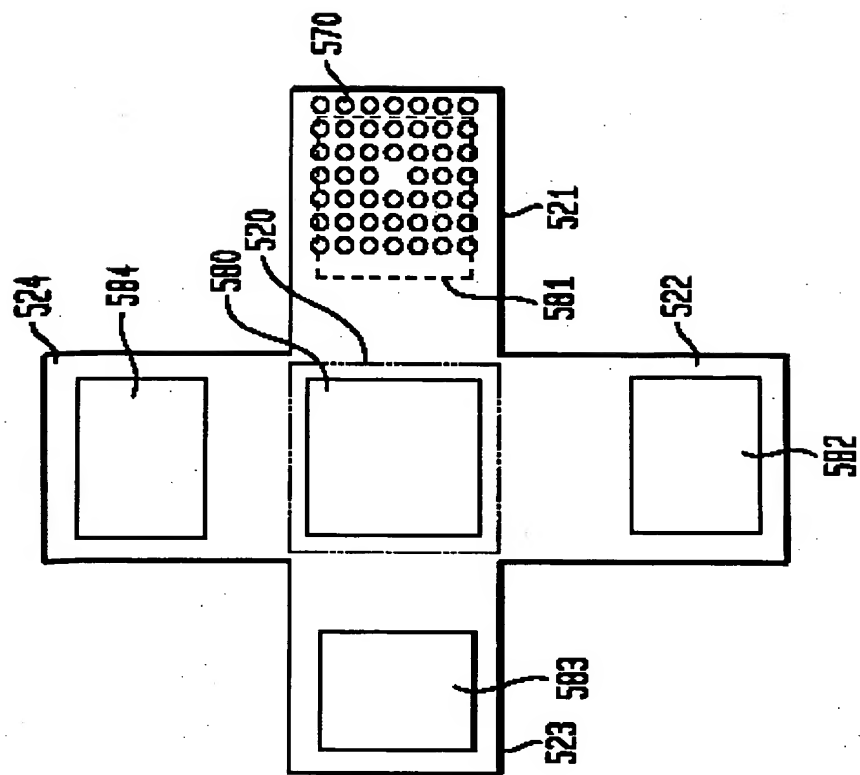


FIG. 11

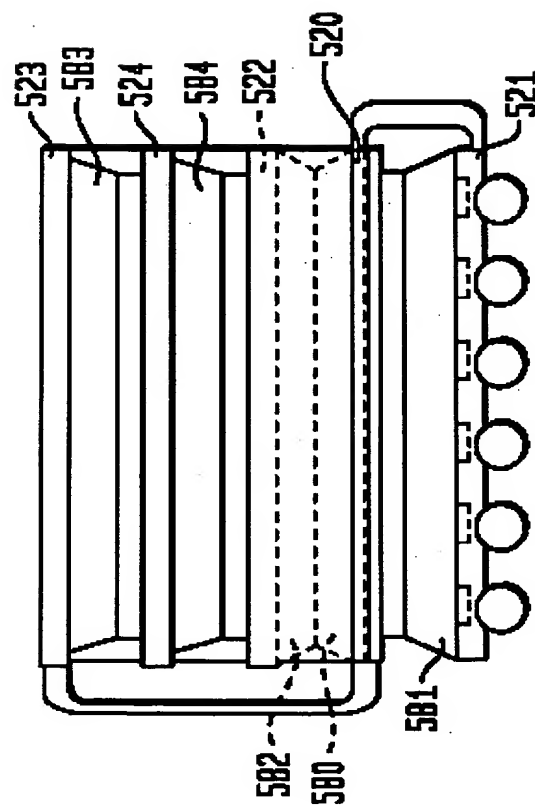


FIG. 12

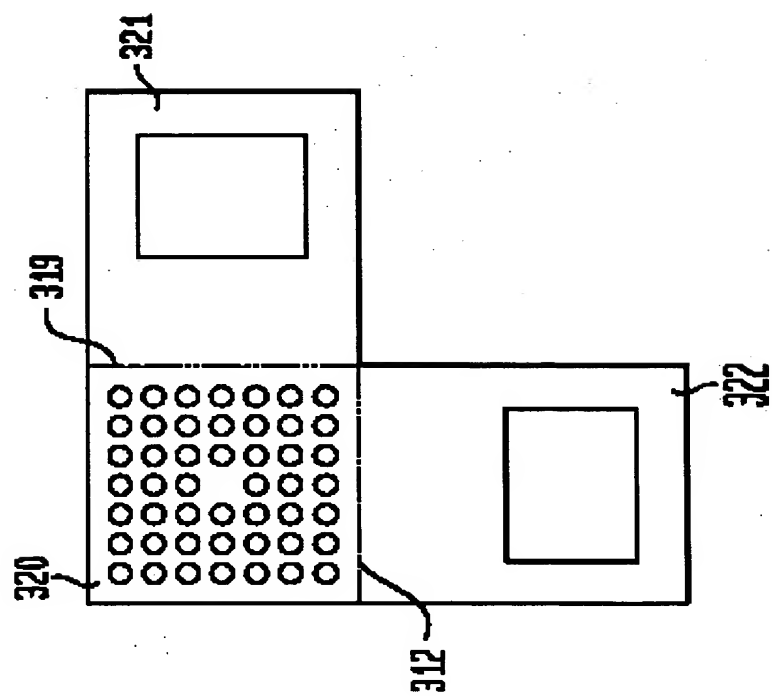


FIG. 13

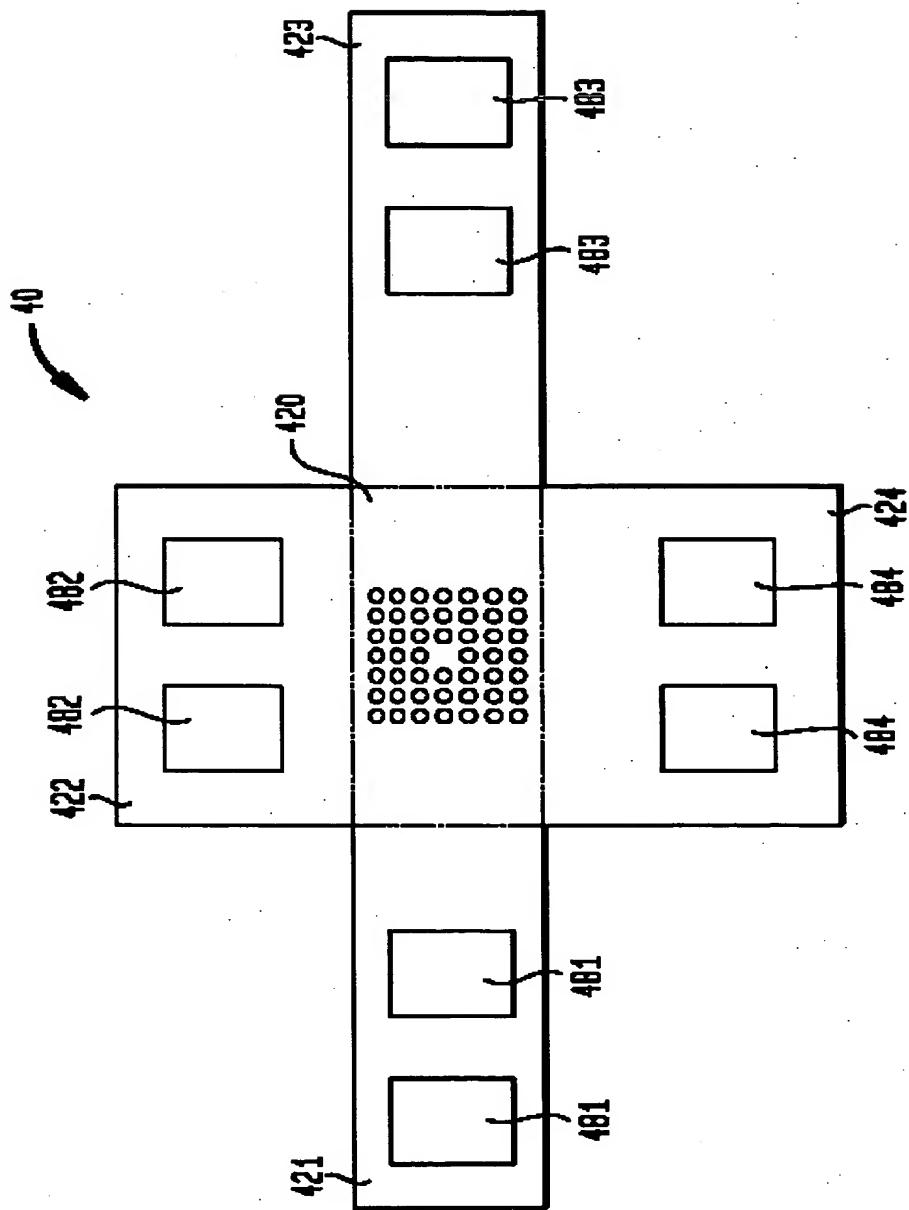


FIG. 14

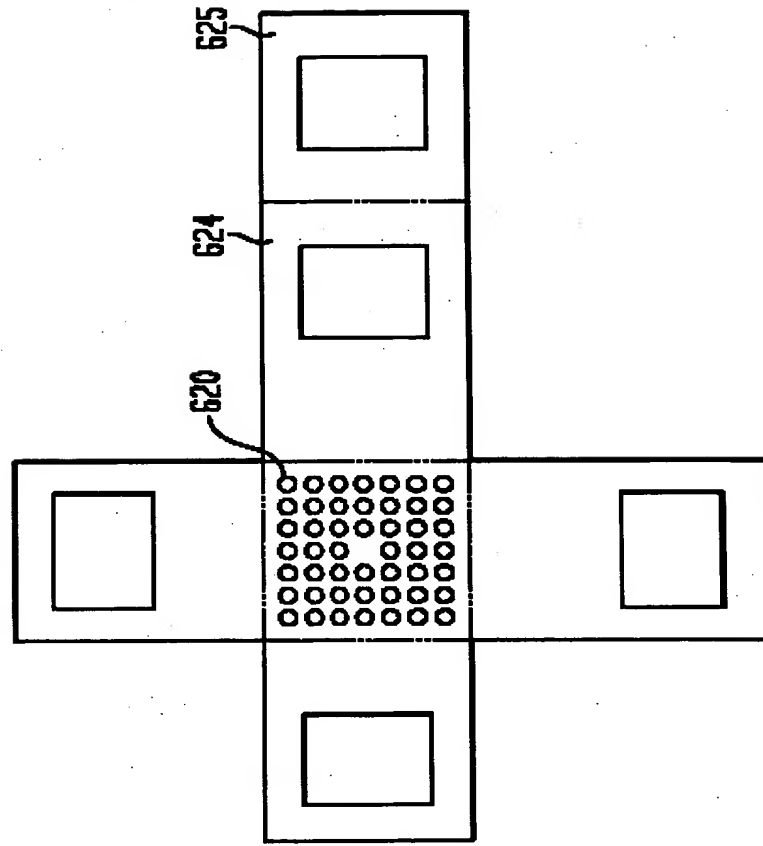


FIG. 15

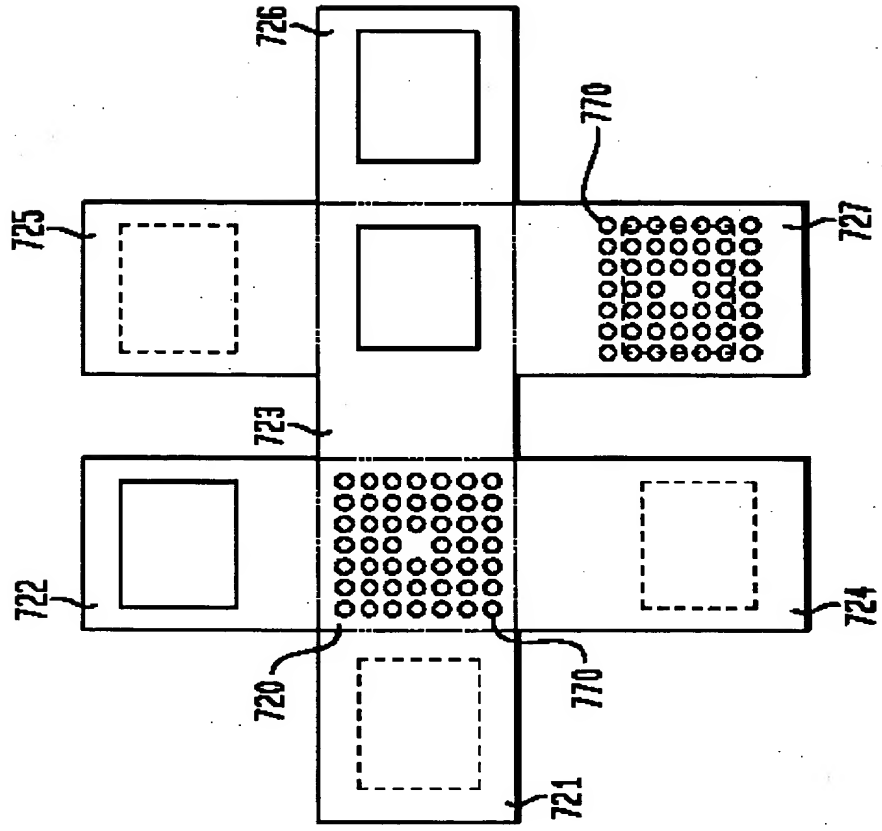


FIG. 16

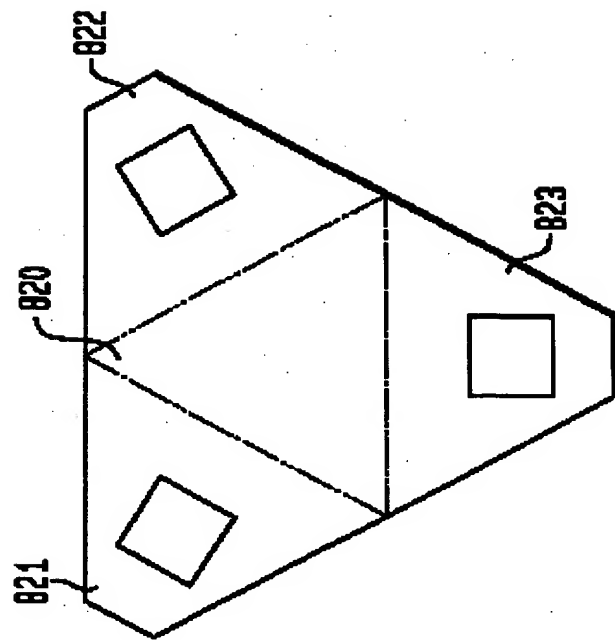




FIG. 17

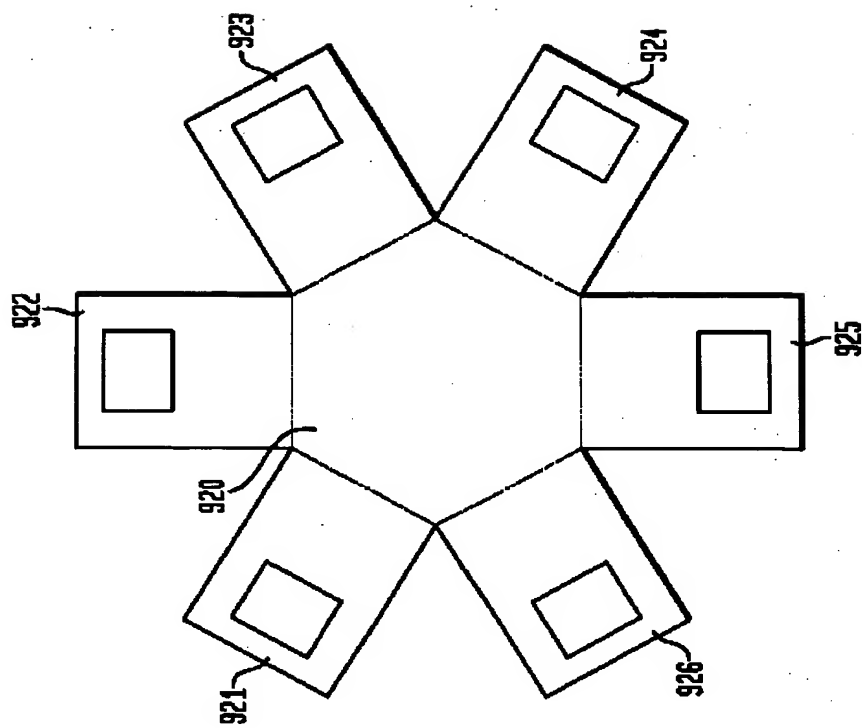


FIG. 18

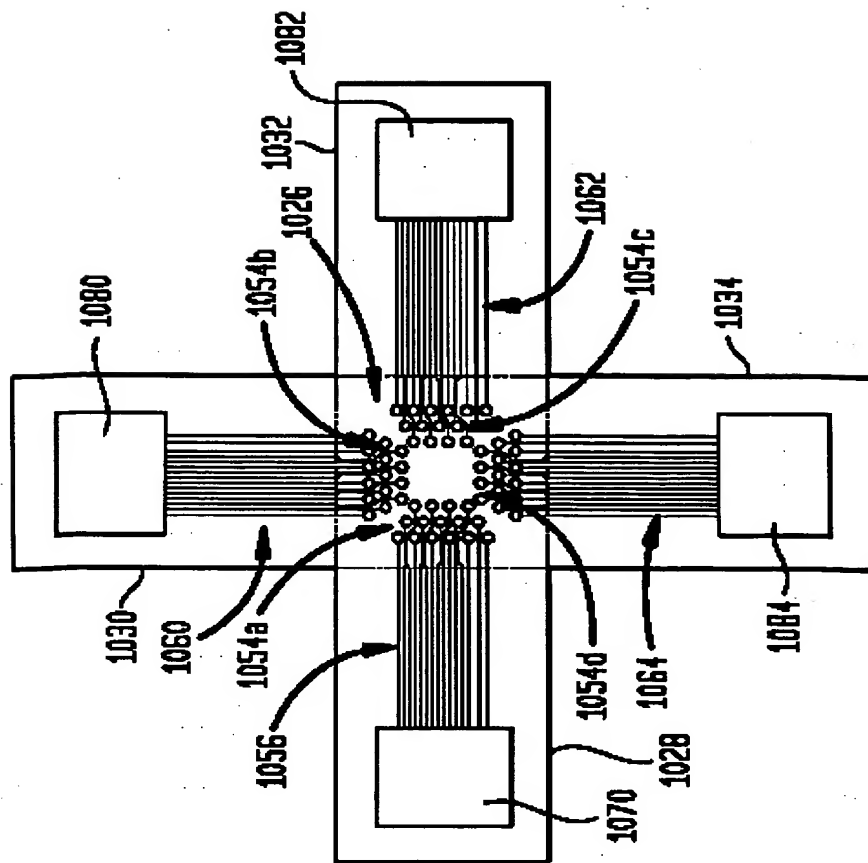
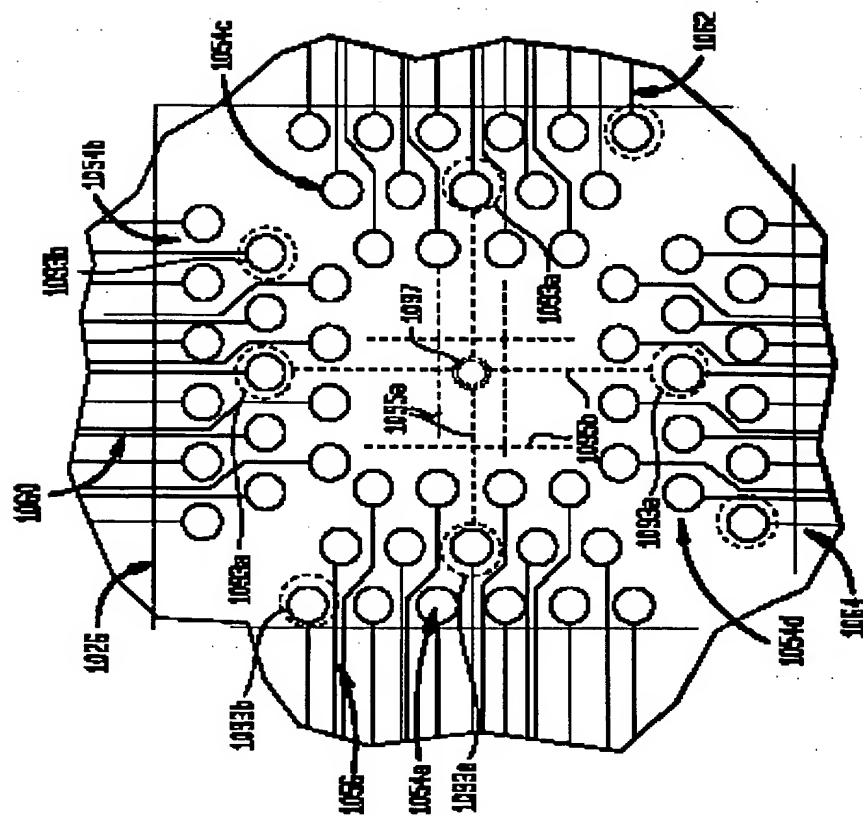


FIG. 19



540

FIG. 20

Top View

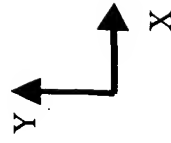
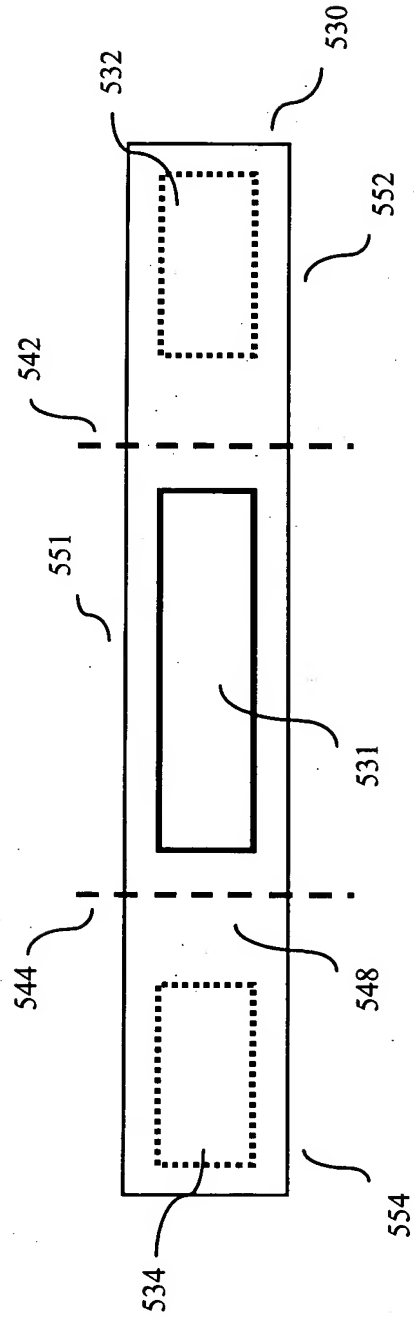


FIG. 21

540

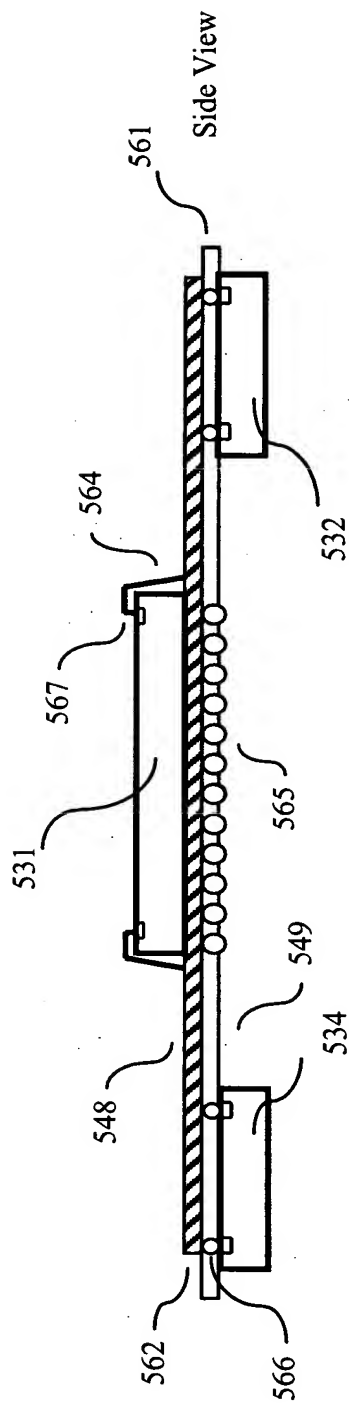
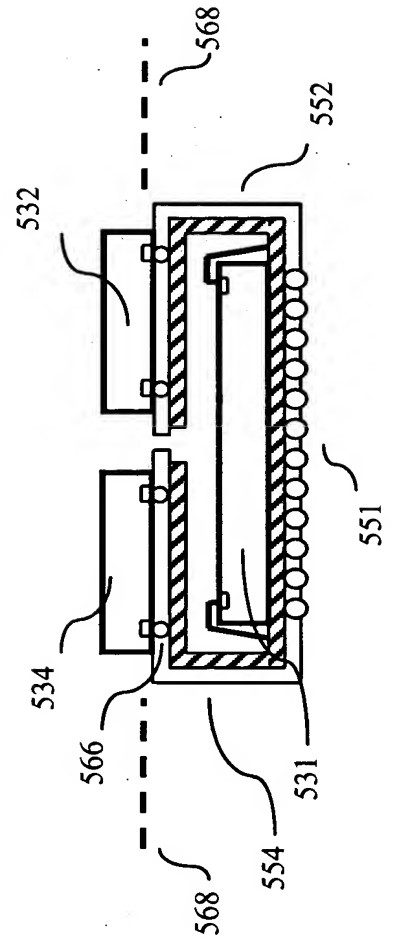


FIG. 22



Side View  
(Folded)

FIG. 23

540

Top View

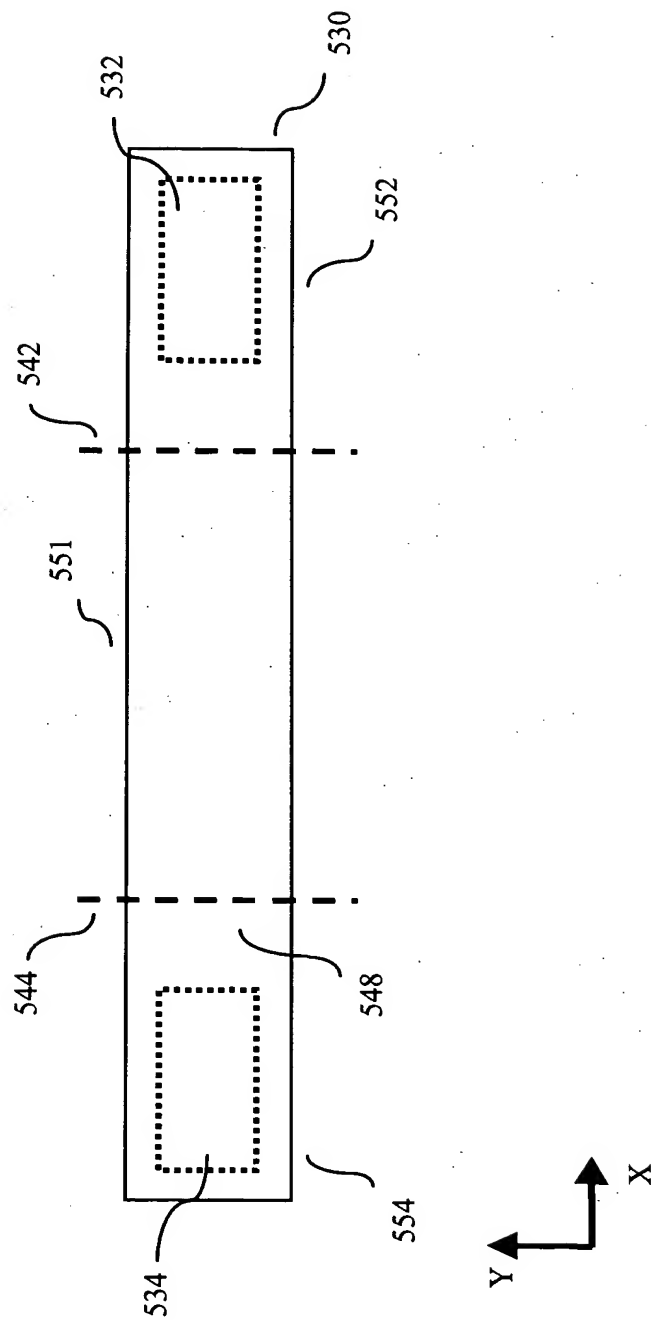


FIG. 24

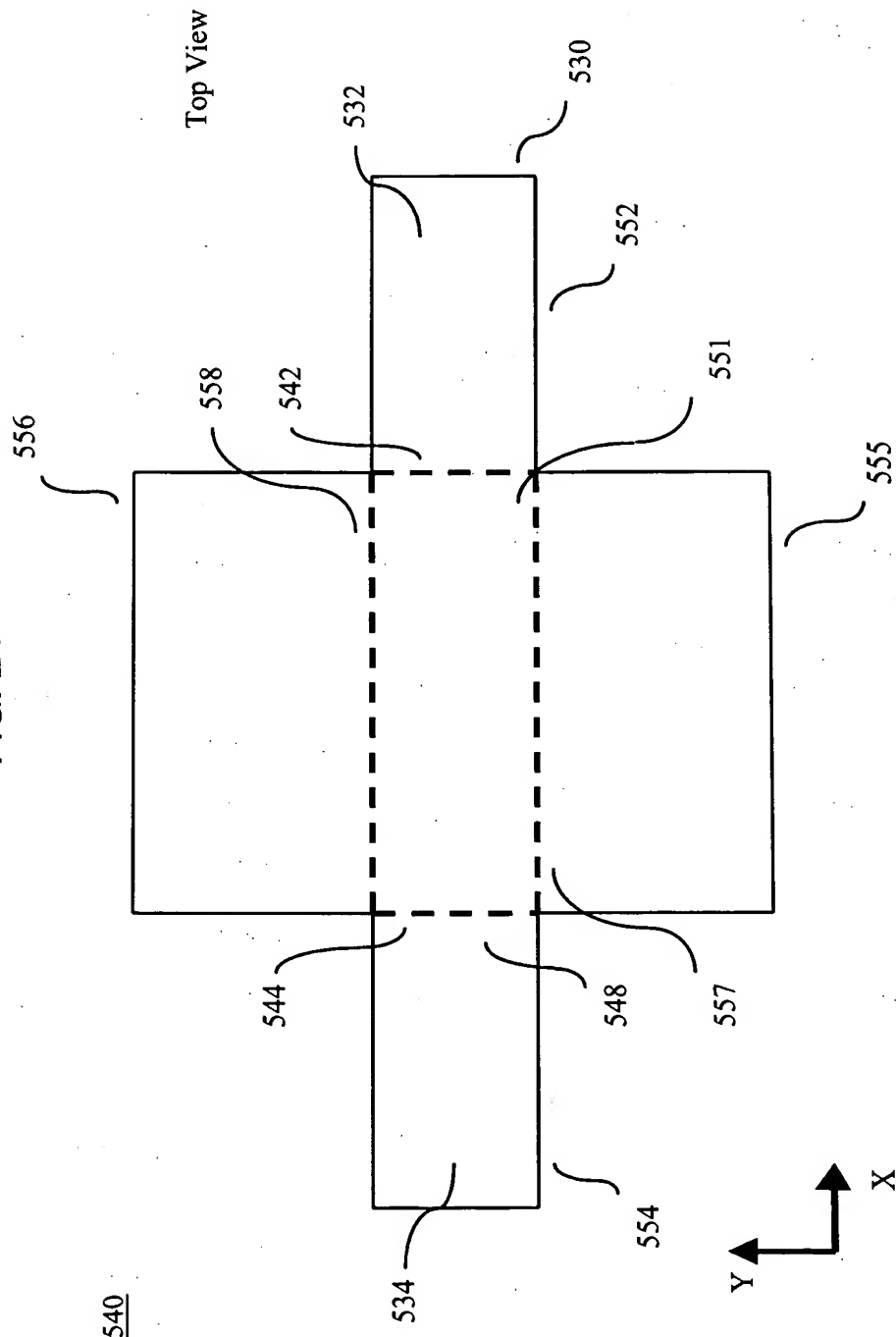




FIG. 25

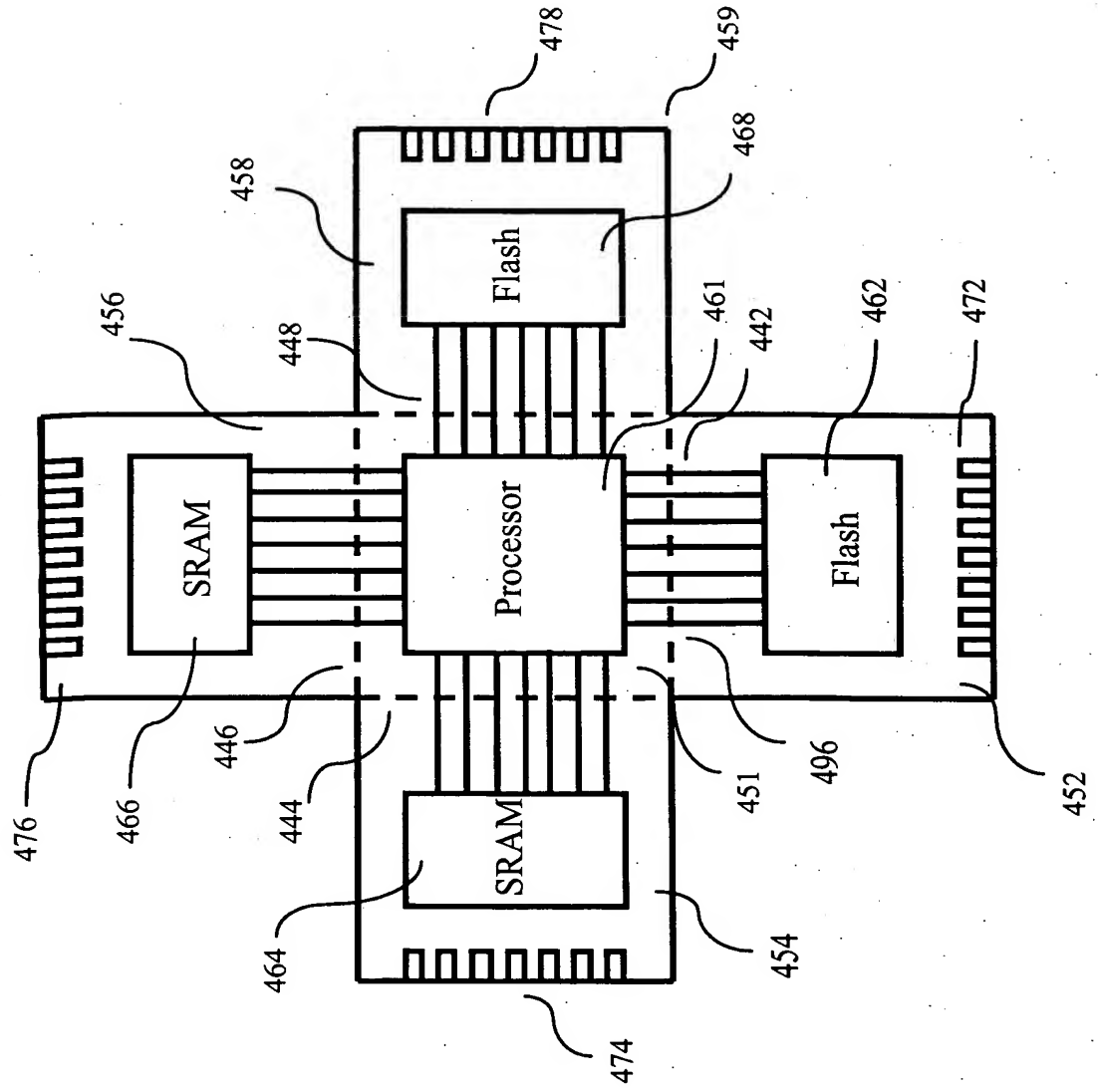


FIG. 26

<u>Usable Packages</u>	<u>Memory Capacity</u>		<u>Failures</u>
	<u>Flash Capacity</u>	<u>SRAM Capacity</u>	
chip assembly 450	32 Mbytes	2 Mbytes	No failures
chip assembly 450-1	16 Mbytes	2 Mbytes	one Flash memory
chip assembly 450-2	32 Mbytes	1 Mbytes	one SRAM memory
chip assembly 450-3	16 Mbytes	1 Mbytes	one Flash and one SRAM

FIG. 27

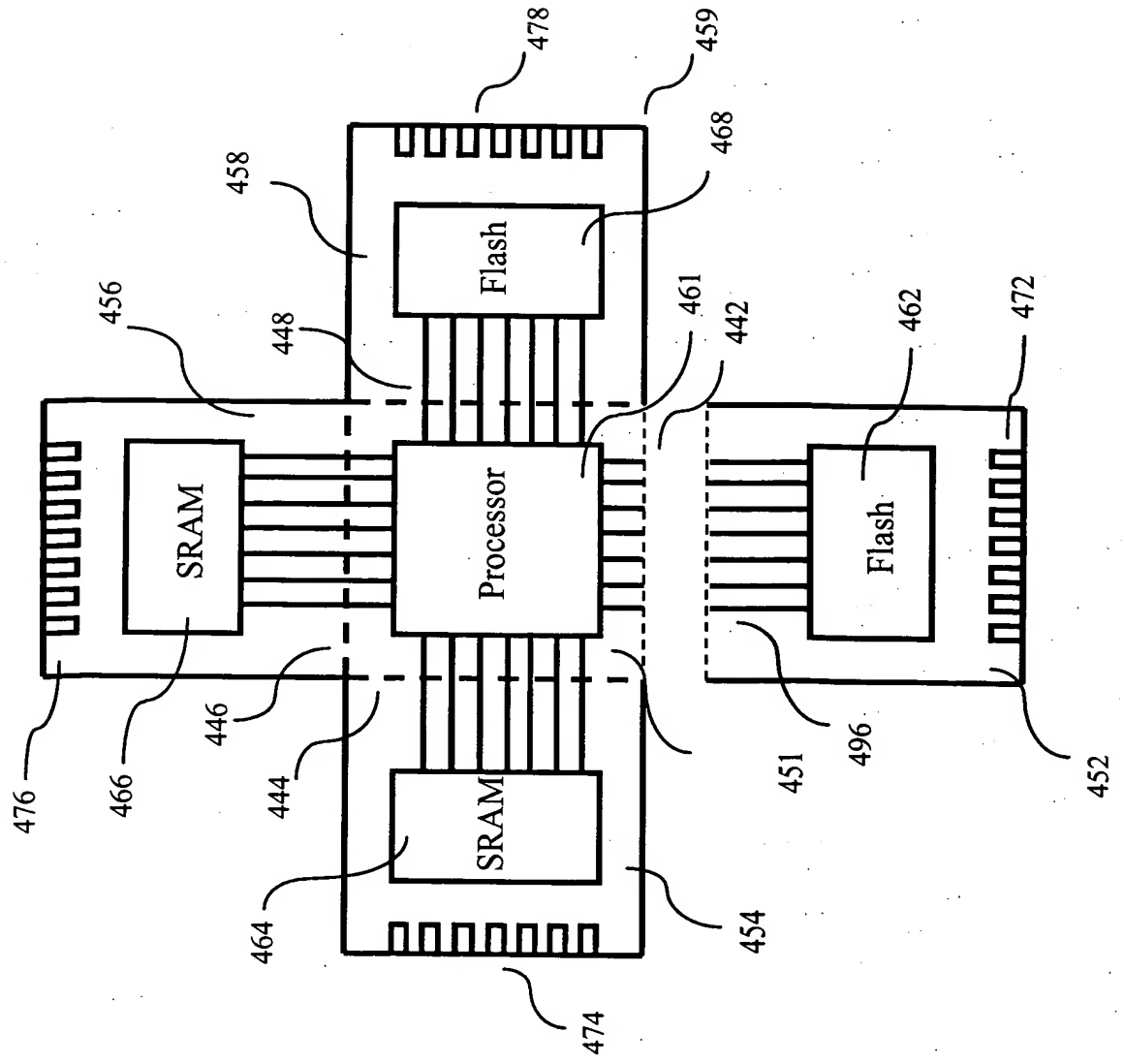
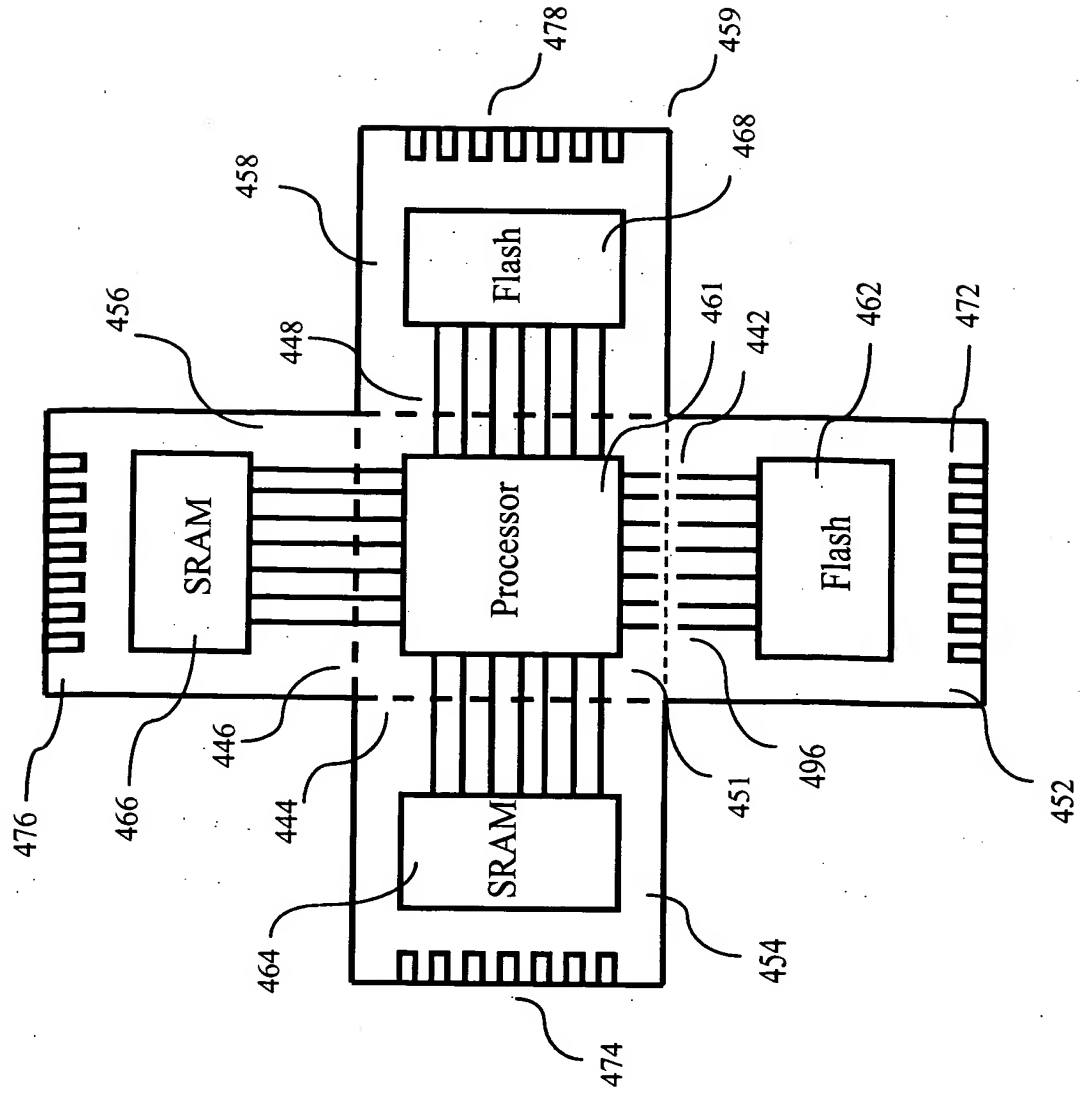


FIG. 28



450

FIG. 29

